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RONALD L. CHICHESTER
BAKER BOTTS L.L.P.
ONE SHELL PLAZA
901 LOUISIANA STREET
HOUSTON, TX 77002-4995

EXAMINER

RAMPURIA, SATISH

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/822,739

Applicant(s)

SIMMERS ET AL.

Examiner

Satish S. Rampuria

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to the application filed on 03/30/2001.
2. Claims 1-17 are pending.

Specification

3. The abstract of the disclosure is objected to because it contains more than 150 words.
Correction is required. See MPEP § 608.01(b).

Claim objections

4. Claims 1, 6, 7, 9, 10, 11, 12, 13, 14, 15, and 16, are objected to because of the following informalities: Claim 1 is missing semicolon “;”on line 8, claim 6, is missing semicolon “;”on line 7, claim 7, is missing semicolon “;”on line 12, claim 9, is missing semicolon “;”on line 2, claim 10, is missing semicolon “;”on lines 10 and 15, claim 11, is missing semicolon “;”on lines 2 and 7, claim 12, is missing semicolon “;”on lines 2 and 7, claim 13, is missing semicolon “;”on lines 2 and 9, claim 14, is missing semicolon “;”on line 2, claim 15, is missing semicolon “;”on line 7, claim 16, is missing semicolon “;”on lines 2 and 9, claim 6, is missing semicolon “;”on line 7.
Appropriate correction is required.

Claim Rejections - 35 USC § 112, second paragraph

5. Claims 1 and 8 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Clarification and/or correction are required.

Regarding, claim 1, on line 3, the limitation, "capable of" is unclear as to the embedded system is being debugged or not being debugged.

Regarding, claim 8, on line 16, the limitation, "single-chip microcontroller" is unclear as to embedded system as whole of claim 7 or a single-chip.

The rejection of the base claim is necessarily incorporated into the dependent claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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7. Claims 1-3, 7-8 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,581,191 to Schubert et al., hereinafter called Schubert.

Per claim 1:

Schubert discloses:

- *An embedded system being debugged* (col. 1, line 19 “debugging of electronic (embedded) system”)
- *a CPU* (col. 45, line 2 Central Processing Unit (CPU))
- *a bus coupled to the CPU, the bus having contents* (col. 33, lines 53-54 “The storage 908 couples to the data bus” see fig. 9)
- *a register, having contents which can be loaded by the CPU* (col. 33, lines 54-55 “store the value at the register output”). It is inherent to load the value by CPU.
- *a debug logic circuit coupled to the bus and to the CPU where the debug logic circuit comprises* (col. 37, lines 8-9 “design control circuit 1400... used to implement temporal logic”). It is inherent to connect the logic circuit to CPU to perform debugging.
- *a breakpoint detect circuit* (col. 4, line 61 “break-points which are detected”) *coupled to the bus and the register* (col. 33, line 60 “bus 918 to drive the input to the register”)
- *a breakpoint signal produced by the breakpoint detect circuit* (col. 4, lines 61-63 “break-points which are detected... circuitry inside the running hardware model”) *when the contents of the register equal the contents of the bus* (col. 5, lines 1-2 “break-points... be made conditioned up on particular values of data-path registers”)

Per claim 2:

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The rejection of claim 1 is incorporated, and further, Schubert discloses:

- ***the bus includes an address bus*** (col. 33, line 56 “the value on an address bus 920 is incremented”)
- ***the register includes a breakpoint address register*** (col. 21, line 24 “registers to physical addresses” and col. 21, lines 6-7 “a break-point database 602 that stores break-points”)
- ***the breakpoint detect circuit is configured to produce the breakpoint signal*** (col. 4, lines 61-63 “break-points which are detected... circuitry inside the running hardware model”) when ***the contents of the address bus equal the contents of the breakpoint address register*** (col. 5, lines 1-2 “break-points... be made conditioned up on particular values of data-path registers”)

Per claim 3:

The rejection of claim 1 is incorporated, and further, Schubert discloses:

- ***the bus includes a data memory address bus and a program memory address bus*** (col. 21, line 24 “registers to physical addresses” and col. 21, lines 6-7 “a break-point database 602 that stores break-points”)
- ***the register includes a breakpoint address register*** (col. 21, line 24 “registers to physical addresses” and col. 21, lines 6-7 “a break-point database 602 that stores break-points”)
- ***the breakpoint detect circuit includes a multiplexer*** (col. 33, lines 48-49 “circuitry 900 includes a register 902, a multiplexer” fig. 9), ***having an output which can be selected to be the contents of the data memory address bus or the program memory address bus*** (col. 33, lines 59-63 “multiplexor selector signal 910 selects the data bus 918 to drive the input to the register 902 via the multiplexor 904, and the selector signal 914 disables the tri-state buffer 906, thereby

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driving the value from the storage 908 into the register 902” fig. 9)

Per claims 7 and 8:

The rejection of claim 1 is incorporated, and further, Schubert does not explicitly disclose:

- a breakpoint counter coupled to the breakpoint detect circuit and responsive to the breakpoint signal for counting the number of breakpoint signals down from a preset number

(col. 46, lines 7-9 “The ICE 2102 monitors... internal portions of the CPU 2002 (for example the instruction pointer counter) to determine whether the program break-point is reached” and col. 37, lines 30-32 “counters operate... loading... value, counting down... loaded value to zero... issuing... event... zero is reached”)

Per claim 17:

Schubert discloses:

- a bus interface for interfacing to a microcontroller bus (col. 40, lines 4-5 “The HDL-based hardware debugger 122 interacts with a user through one or more user interfaces and interacts with the DIC 106 through a host communication controller”)

- a communications interface for receiving debug instructions (col. 45, lines 23-24 “The ICE 2102 interfaces the software debugger 2004 with the CPU 2002”)

- a register, having contents which can be loaded through the communications interface (col. 33, lines 1-2 “A communication controller 816 couples to the status registers 812 and the configuration registers 814”)

- *a breakpoint detect circuit* (col. 4, line 61 “break-points which are detected”) *coupled to the bus and the register* (col. 33, line 60 “bus 918 to drive the input to the register”)
- *and a breakpoint signal produced by the breakpoint detect circuit* (col. 4, lines 61-63 “break-points which are detected... circuitry inside the running hardware model”) *when the contents of the register equal the contents of the bus* (col. 5, lines 1-2 “break-points... be made conditioned up on particular values of data-path registers”)

Substantially as claimed.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schubert, in view of JP 59163653 A to TAKAGI et al., hereinafter called TAKAGI.

Per claim 4:

The rejection of claim 3 is incorporated, and further, Schubert discloses:

- *the breakpoint detect circuit* (col. 4, line 61 “break-points which are detected”) *includes an address comparator* (col. 34, lines 38-39 “The mode of the comparator 1006 can be controlled by a configurable trigger comparison register”)

- the comparator producing a data-memory-address-equal signal (col. 34, lines 36-37 “trigger register... stores a trigger value... compared to monitored signal”)

- the output of the multiplexer is selected to be the contents of the data memory address bus and the output of the multiplexer equals the contents of the breakpoint address register (col. 33, lines 59-63 “multiplexor selector signal 910 selects the data bus 918 to drive the input to the register 902 via the multiplexor 904, and the selector signal 914 disables the tri-state buffer 906, thereby driving the value from the storage 908 into the register 902” fig. 9)

Schubert does not explicitly disclose comparator coupled to the output of the multiplexer and the breakpoint address register.

However, TAKAGI discloses in an analogous computer system comparator coupled to the output of the multiplexer and the breakpoint address register (page 1, section “Constitution- multiplexer 3, a comparator 5 and a break point control circuit 7 of a debug device 1 are connected to the buses 12&sim14, respectively”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the system with coupled comparator, multiplexer, and breakpoint address register as taught by TAKAGI into the system of debugging embedded systems as taught by Schubert. The modification would be obvious because of one of ordinary skill in the art would be motivated have system with coupled comparator, multiplexer, and breakpoint address register to avoid the generation of useless break operation as suggested by TAKAGI (page 1, section “Purpose- To avoid... computer system”).

Per claim 5:

The rejection of claim 3 is incorporated, and further, Schubert discloses:

- the breakpoint detect circuit includes a compare circuit (col. 4, line 61 “break-points which are detected”) includes a comparator circuit (col. 34, lines 38-39 “The mode of the comparator 1006 can be controlled by a configurable trigger comparison register”) **a read signal, a write signal, and a data read/write signal** (col. 27, lines 55-56 “a break-point analysis module 1712 then reads the trigger detection circuitry” and col. 28, lines 32-33 “writer module 1720 also reads in the original HDL description 304”) **the compare circuit producing an address-equal-on-read signal** (col. 34, lines 36-37 “trigger register... stores a trigger value... compared to monitored signal”)

- the output of the multiplexer is selected to be the contents of the data memory address bus; and the output of the multiplexer equals the contents of the breakpoint address register (col. 33, lines 59-63 “multiplexor selector signal 910 selects the data bus 918 to drive the input to the register 902 via the multiplexor 904, and the selector signal 914 disables the tri-state buffer 906, thereby driving the value from the storage 908 into the register 902” fig. 9)

- the read signal has been asserted; and the data read/write signal has been asserted (col. 23, lines 38-42 “The file-based DI criteria... directly read by... DI manager 732... stores selections of trigger conditions into the trigger condition database 718 and stores selections of signal values to be made visible and/or patchable into the signal database 722”)

- the compare circuit producing an address-equal-on-write signal (col. 34, lines 36-37 “trigger register... stores a trigger value... compared to monitored signal”) **the output of the multiplexer is selected to be the data memory address bus; the output of the multiplexer**

equals the contents of the breakpoint address register (col. 33, lines 59-63 “multiplexor selector signal 910 selects the data bus 918 to drive the input to the register 902 via the multiplexor 904, and the selector signal 914 disables the tri-state buffer 906, thereby driving the value from the storage 908 into the register 902” fig. 9)

- the write signal has been asserted; and the data read/write signal has been asserted (col. 28, lines 31-36 “DIC writer module 1720 also reads... original HDL description 304... information... from... design database 712... DIC database 736... writes out... HDL description 316”)

- where the breakpoint detect circuit (col. 4, line 61 “break-points which are detected”) *is configured to produce the breakpoint signal* (col. 5, lines 1-2 “break-points can be made conditioned upon particular values of data-path registers”) *when a data-value-compare-select signal is not asserted and the compare circuit has produced either the address-equal-on-read signal or the address-equal-on-write signal* (col. 34, lines 35-38 “trigger detection circuit 1000 includes a configurable trigger register (TR) 1002... stores a trigger value... compared to ... signal (ISR) 1004 by a comparator 1006” and col. 34, lines 38-41 “the comparator 1006... controlled by a configurable trigger comparison register (TCR) 1008... different comparison modes are test for equivalence, test for smaller-than”)

Schubert does not explicitly disclose comparator coupled to the output of the multiplexer and the breakpoint address register.

However, TAKAGI discloses in an analogous computer system comparator coupled to the output of the multiplexer and the breakpoint address register (page 1, section “Constitution-

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multiplexer 3, a comparator 5 and a break point control circuit 7 of a debug device 1 are connected to the bus”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the system with coupled comparator, multiplexer, and breakpoint address register as taught by TAKAGI into the system of debugging embedded systems as taught by Schubert. The modification would be obvious because of one of ordinary skill in the art would be motivated have system with coupled comparator, multiplexer, and breakpoint address register to avoid the generation of useless break operation as suggested by TAKAGI (page 1, section “Purpose- To avoid... computer system”).

Per claim 6:

The rejection of claim 5 is incorporated, and further, Schubert discloses:

- ***the register includes a breakpoint data register*** (col. 21, line 24 “registers to physical addresses” and col. 21, lines 6-7 “a break-point database 602 that stores break-points”)
- ***the bus includes a data memory data bus*** (col. 33, lines 53-55 “The storage 908 couples to the data bus 918... store the value at the register output 916”)
- ***the debug logic circuit*** (col. 37, lines 8-9 “design control circuit 1400... used to implement temporal logic”) ***includes a data comparator*** (col. 34, lines 36-37 “a trigger value... compared... by a comparator 1006”) ***coupled to the breakpoint data register*** (col. 21, lines 6-7 “a break-point database 602 that stores break-points”) ***and the data memory data bus*** (col. “The storage 908 couples to the data bus 918... store the value at the register output 916”) ***which produces a data-equal signal when the contents of the data memory data bus equal the***

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contents of the breakpoint data register (col. 5, lines 1-2 “break-points can be made conditioned upon particular values of data-path registers”)

- where the breakpoint detect circuit is configured to produce the break signal when the data-value-compare-select signal is asserted, the data-equal signal is produced, and the compare circuit has produced either the address-equal-on-read signal or the address-equal-on-write signal (col. 34, lines 35-38 “trigger detection circuit 1000 includes a configurable trigger register (TR) 1002... stores a trigger value... compared to ... signal (ISR) 1004 by a comparator 1006” and col. 34, lines 38-41 “the comparator 1006... controlled by a configurable trigger comparison register (TCR) 1008... different comparison modes are test for equivalence, test for smaller-than”)

10. Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schubert, in view of US Patent No. 5,943,498 to Yano et al., hereinafter called Yano.

Per claim 9:

Schubert discloses:

- A method for debugging an embedded system (col. 5, lines 58-59 “system for analysis, diagnosis and debugging fabricated hardware designs”) *comprising a microcontroller, the microcontroller comprising a CPU* (col. 9, lines 15- 21 ““Central Processing Unit” or “CPU”... microprocessors”)

- running an application software on the microcontroller. It is inherent to run an application to debug for any errors.

- ***detecting the predetermined condition*** (col. 45, lines 38-40 “a trigger condition set... detected at the run-time in the DIC”)
- ***interrupting the CPU*** (col. 45, line 64 “software program... halts the program’s execution”)
- ***providing the ability to view the condition of the microcontroller*** (col. 45, lines 13-14 “program break-points define the condition... program execution is halted... designer can examine... operation of the software program”)

Schubert does not explicitly disclose programming a debug logic circuit residing on the same chip as the microcontroller.

However, Yano discloses in an analogous computer system programming a debug logic circuit residing on the same chip as the microcontroller (col. 1, lines “the logic circuits for running monitor programs in the monitor memory in the debugging tool, the logic circuits for performing execution control including hardware break points, and the logic circuits for outputting the PC information of the executed instructions are incorporated in the microprocessor”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of programming the logic circuits as taught by Yano into the method of debugging system as taught by Schubert. The modification would be obvious because of one of ordinary skill in the art would be motivated program the debug logic circuit on the same microcontroller to save time and accurately debug the system as suggested by Yano (col. 2, lines 25-39).

Per claims 10 and 11, 12, 13, 16:

Schubert discloses:

The rejection of claim 9 is incorporated, and further, Schubert discloses:

- *storing a breakpoint address in a breakpoint address register* (col. 21, line 24 “registers to physical addresses” and col. 21, lines 6-7 “a break-point database 602 that stores break-points”)

- *selecting a program memory address bus to compare to the contents of the breakpoint address register* (col. 28, lines 19-21 “a DIC register-to-physical mapping module 1718 maps each register configuration and each status register in the DIC into an address space of physical memory”)

- *and setting a breakpoint count register to 0* (col. 37, lines 30-32 “counters operate... loading... value, counting down... loaded value to zero... issuing... event... zero is reached”)

- *detecting and interrupting* (col. 4, lines 61-63 “break-points which are detected comprise, comparing (col. 34, lines 36-37 “a trigger value... compared... by a comparator 1006”) *the contents of the program memory address bus to the contents of the breakpoint register; and if they are equal* (col. 28, lines 19-21 “a DIC register-to-physical mapping module 1718 maps each register configuration and each status register in the DIC into an address space of physical memory”), *interrupting the CPU* (col. 45, line 64 “software program... halts the program’s execution”)

Per claims 14 and 15:

Schubert discloses:

The rejection of claim 13 is incorporated, and further, Schubert discloses:

- *specifying that the breakpoint is to occur on a write* (col. 19, lines 45-48 “The break-point information comprises the HDL location of the selected break-point, and the current status type... the status type for a selected break-point is "selected"”)

- *and comparing the contents of the data memory address bus to the contents of the breakpoint address register comprises performing the compare on a write* (col. 28, lines 19-21 “a DIC register-to-physical mapping module 1718 maps each register configuration and each status register in the DIC into an address space of physical memory”), *interrupting the CPU* (col. 45, line 64 “software program... halts the program’s execution”)

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent is cited to further show the state of the art with respect to ***.

US Patent No. 6,618,839 to Beardslee et al.

US Patent No. 5,915,083 to Ponte

European Patent No. EP 0 862 116 A2 to Ponte et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Satish S. Rampuria whose telephone number is 703-305-8891.

The examiner can normally be reached on 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria

Patent Examiner

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04/19/2004

Kakali Chaki

**KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100**